Amendments to the Specification:

Please replace the paragraph beginning at page 2, line 16, with the following rewritten paragraph:

The present invention aims to overcome the above limitations of the current state of the art, and to propose a signal for conversion of a received PWM signal which can be made entirely in integrated technology, while eliminating problems of variation of period in the PWM signal, and at the same time being capable in all cases of delivering with precision the voltage represented by the PWM signal.

According to a first aspect of the invention, an alternator for a motor vehicle, comprising a rotor and a stator and a regulator circuit for varying the excitation of the alternator by comparison of a signal representing the output voltage of the alternator with a variable reference voltage, and a conversion circuit ~~adapted~~ provided to vary the ~~said~~ reference voltage as a function of a reference control signal in the form of a pulse width modulated signal, is ~~characterised~~ characterized in that the conversion circuit comprises, in combination:

- an internal clock with a controllable variable period;
- a differential circuit ~~adapted~~ provided to establish a difference signal between the period of the reference control signal and the period of a signal from the internal clock;
- a control circuit for the internal clock, adapted to control the internal clock in response to the ~~said~~ difference signal in such a way as to ~~equalise~~ equalize the period of the internal clock signal

and the period of the ~~said~~ control signal; and

- a circuit for converting pulse width into voltage, comprising a counter which is paced by the ~~said~~ controllable internal clock and which is adapted to perform a counting operation so long as the ~~said~~ reference control signal is at a given logic level, and a digital/analogue converter which is adapted to convert a value of the count supplied by the ~~said~~ counter into a voltage from which the reference voltage of the regulator is obtained.

Please replace the paragraph beginning at page 3, line 18, with the following rewritten paragraph:

According to the invention in a second aspect, an interface device for constituting the interface between a control apparatus which supplies a reference control signal in the form of a pulse width modulated signal, and a regulating device for a motor vehicle alternator, wherein the variations in width of the pulses in the ~~said~~ signal are arranged to be converted into variations in a reference voltage of the ~~said~~ regulating device, is ~~characterised~~ characterized in that it comprises, in combination:

- an internal clock with a controllable variable period;
- a differential circuit adapted to establish a difference signal between the period of the reference control signal and the period of a signal from the internal clock;
- a control circuit for the internal clock, adapted to control the internal clock in response to the

~~said~~ difference signal in such a way as to ~~equalise~~ equalize the period of the internal clock signal and the period of the ~~said~~ control signal; and

- a circuit for converting pulse width into voltage, comprising a counter which is paced by the ~~said~~ controllable internal clock and which is adapted to perform a counting operation so long as the ~~said~~ reference control signal is at a given logic level, and a digital/analogue converter which is adapted to convert a value of the count supplied by the ~~said~~ counter into a voltage from which the reference voltage of the regulator is obtained.

Please replace the paragraph beginning at page 4, line 21, with the following rewritten paragraph:

The difference circuit may comprise a means for producing pulses representing the difference between the ~~said~~ symmetrical rectangular signal and a signal produced from the internal clock.

Please replace the paragraph beginning at page 4, line 24, with the following rewritten paragraph:

The width of the difference pulses may be proportional to the difference between the period of the reference control signal and the period of the ~~said~~ signal from the internal clock.

Please replace the paragraph beginning at page 5, line 1, with the following rewritten paragraph:

The difference circuit may include a means for producing a signal representing difference in direction, at least during the duration of the ~~said~~ difference pulses.

Please replace the paragraph beginning at page 5, line 4, with the following rewritten paragraph:

The control circuit for the internal clock may comprise a bidirectional counter adapted to receive the ~~said~~ difference pulses and the ~~said~~ direction difference signal, together with a digital/analogue converter receiving the output from the ~~said~~ bidirectional counter.

Please replace the paragraph beginning at page 5, line 9, with the following rewritten paragraph:

The digital/analogue converter of the ~~said~~ conversion circuit may have a ~~memorisation~~ memorization input, while means may be provided for applying to the ~~said~~ input a ~~memorisation~~ memorization signal during which the ~~said~~ reference control signal is at a logic level other than the ~~said~~ given logic level, each time that the ~~said~~ counter has performed an acquisition of the value of the cyclic ratio of the reference control signal.

Please replace the paragraph beginning at page 6, line 14, with the following rewritten paragraph:

Figures 8 and 9 show, respectively, two concrete embodiments of two further blocks in the diagram shown in Figure 4, which enable the cyclic ratio of the reference control signal to be measured after the internal clock has been ~~synchronised~~ synchronized with the ~~said~~ reference control signal.

Please replace the paragraph beginning at page 9, line 4, with the following rewritten paragraph:

The multi-bit output of the counter CT2 is applied to a second digital/analogue converter CNA2, the output of which is an analogue voltage Vcorr, which is adapted to correct a fixed voltage also produced (in a manner known *per se*) in the regulator of the alternator, so as to obtain the variable reference voltage Vref. The converter CNA2 has an input MEM which enables the value available at the output of the counter CT2 to be taken and ~~memorised~~ memorized. This input MEM is connected to the output of the logic circuit L5, one of the inputs of which is connected to the PWM input of the logic circuit L1, while another input is connected to the output ERR of the logic circuit L1.

Please replace the paragraph beginning at page 10, line 3, with the following rewritten paragraph:

The gate XOR thus delivers an inverted error signal INVERR which converts an error in ~~synchronisation~~ synchronization between the frequency of the signal CKV delivered by the clock VCO and the frequency of the reference control signal PWM. This inverted error signal INVERR is applied on the holding input of the bidirectional counter CTDC. This counter counts up or down according to the level of the signal C/D provided by the logic circuit L2, and it does this over the whole duration of the inverted error signal INVERR. The output of the counter CTDC is coded on 8 bits and is converted into an analogue signal by the converter CNA1. The analogue signal is applied to the input of the variable clock signal VCO, the oscillation frequency of which varies in such a way that it seeks to annul the error signal.

Please replace the paragraph beginning at page 11, line 4, with the following rewritten paragraph:

It is desirable to provide an output circuit CNA2 with a continuous voltage, avoiding conversion of the output values from the counter CT2 during the counting and zeroing phases. The digital/analogue conversion has to be carried out when the counter CT2 has just measured the pulse width of the PWM signal representing the cyclic ratio of that signal. To this end, the circuit CNA2 is chosen to be of the type having a sampling input (or ~~memorising~~ memorizing

input) CE, which enables the output voltage to be blocked at the current value when the logic signal MEM on that input is at logic level 0. The logic circuit L5 is designed to produce the signal MEM from the PWM signal and the signal ERR, whereby to obtain a continuous output voltage of the converter CNA2.

Please replace the paragraph beginning at page 12, line 13, with the following rewritten paragraph:

Due to the fact that the period of the PWM signal and the period of the clock signal VCO are not synchronous (the period of the PWM signal being variable), this means that the counter CT1/Ctb will finish being incremented before or after the end of the period Tpwm of the PWM signal. It also means that such an offset represents the ~~synchronising~~ synchronizing error that exists. This error is revealed first by combining the signal on the output q7 of Ctb with the signal RAZ, in the NOR gate NOR3, and then by combining the output of this gate with the error signal ERR delivered by the counter Cta into the gate XOR, which delivers the required error signal INVERR.

Please replace the paragraph beginning at page 15, line 4, with the following rewritten paragraph:

In this situation, the transistor T4 is ~~polarised~~ polarized inversely and is therefore blocked, while the diode D is passing. The current I produced by T3 is therefore able to flow through the diode D, and accordingly there is a current I/2 in the transistor T6 and the resistor R7, and a current I/2 in the capacitor C.

Please replace the paragraph beginning at page 15, line 9, with the following rewritten paragraph:

The capacitor C therefore charges up, and when the inversion threshold of the operational amplifier A3 is reached, the output of the latter passes to zero potential with a low inversion threshold. The transistor T4 then becomes passing and the diode D, ~~polarised~~ polarized inversely, becomes blocked. The current arising from the transistor T3 is then no longer able to pass through the diode D, and it flows through the transistor T4 which is connected to ground. The capacitor C then discharges via the current source constituted by the components T6, A2 and R7.

Please replace the paragraph beginning at page 23, line 1, with the following rewritten paragraph:

~~AN ALTERNATOR EQUIPPED WITH IMPROVED INTERFACE MEANS BETWEEN AN ENGINE CONTROL APPARATUS AND ITS REGULATOR CIRCUIT, AND A CORRESPONDING INTERFACE~~

ABSTRACT ~~OF THE DISCLOSURE~~

A motor vehicle alternator includes a regulator for varying excitation as a function of a reference variable, together with a conversion circuit for varying the reference variable (such as a voltage) according to a PWM signal. It includes, in combination: an internal clock with a controlled variable period; a difference circuit which produces a difference signal between the period of the PWM signal and that of a signal from the clock; a control circuit which governs the internal clock in response to the difference signal in such a way as to ~~equalise~~ equalize the periods of the internal clock signal and the PWM signal; and a conversion circuit which comprises a counter paced by the clock and active while the PWM signal is at a given logic level, together with a D/A converter for converting the count from the counter into a voltage from which the regulator reference voltage is obtained.